

### About SmartMesh IA-510

Dust Networks' SmartMesh® IA-510 is a WirelessHART®-compliant system that offers industrial automation vendors an industry-leading standards-based system that delivers flexible, secure solutions. The SmartMesh IA-510 system's Intelligent Networking Platform delivers dynamic network optimization and intelligent routing to achieve the carrier-class data reliability, lower latency, and deterministic power management required for the industrial automation market. The SmartMesh IA-510 system consists of the PM2511 embedded network manager and two mote form factors: the DN2510 Mote-on-Chip™ (MoC) and the M2510 RF-certified mote module. SmartMesh IA-510 systems are easy for industrial automation vendors to integrate and simple for end users to deploy.

### Product Description—DN2510

The WirelessHART-compliant DN2510 MoC combines Dust Networks' robust, Intelligent Networking Platform and industry-leading low-power radio technology in an easy-to-integrate 12 mm x 12 mm System-in-Package (SiP). As part of the SmartMesh IA-510 system, the DN2510 provides industrial automation vendors with a complete embedded wireless sensor networking solution for WirelessHART applications that assures multivendor interoperability and offers forward compatibility.

The DN2510 is tailored for use in battery-powered and energy-scavenging wireless devices for applications that demand proven performance and scalability. With Dust Networks' innovative IEEE 802.15.4-compliant design and power amplifier, the DN2510 enables a decade of battery life on two AA batteries. Additionally, all motes can function as both battery-powered routers and nodes, enabling a full mesh topology that provides more redundant routes and higher performance.

The network-ready MoC integrates all radio circuitry components, eliminating the burden of complex RF design—requiring only a simple antenna connector for robust wireless connectivity. The fully engineered RF solution, comprehensive APIs, and complete development documentation for the DN2510 MoC offer rapid field device integration, reduced development time, and reduced cost for WirelessHART solutions.

### Key Product Features

#### WirelessHART Compliance

- Interoperable with WirelessHART devices

#### Superior Reliability

- Robust network reliability in even the most challenging industrial environments
- Every DN2510 can act as both an endpoint and a router, increasing network reliability

#### Easy Integration

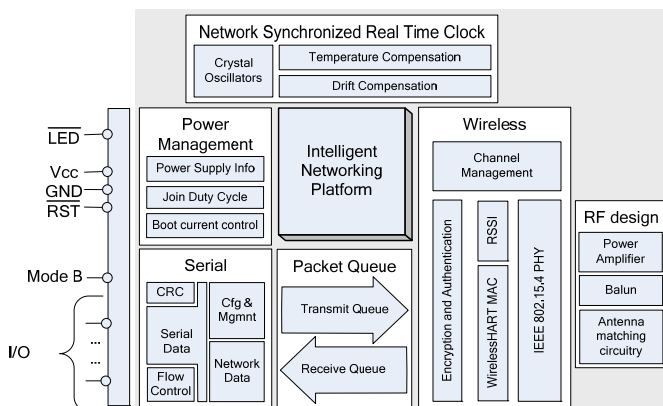
- Fully-engineered RF—power amplifier, balun, crystals, and antenna matching circuitry in an ultra-compact 12 x 12 mm size
- Comprehensive APIs deliver rich functionality and flexibility without complex coding

#### Ultra-low Power Consumption

- Industry-leading radio technology optimized for battery or loop-powered operation
- Ultra-efficient power usage, enabled through SmartMesh Intelligent Network management, delivers over a decade of network operation on two AA batteries

#### Secure Global Market Solution

- IEEE 802.15.4-certified radio operates on 2.4 GHz global license-free band
- Configurable radio output power—meets RF emission limits for different regions with a single product
- AES-128 bit encryption (certified NIST FIPS-197 compliant)



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## 1.0 Absolute Maximum Ratings

The absolute maximum ratings shown below should not be violated under any circumstances. Permanent damage to the device may be caused by exceeding one or more of these parameters.

Unless otherwise noted, all voltages in Table 1 are made relative to  $V_{SS}$ .

**Table 1 Absolute Maximum Ratings**

Parameter	Min	Typ	Max	Units	Comments
Supply voltage ( $V_{DD}$ to $V_{SS}$ )	-0.3		3.6	V	
Voltage on any digital I/O pin	-0.3		$V_{DD} + 0.3$ up to 3.6	V	
Input RF level			10	dBm	Input power at antenna connector
Storage temperature range	-40		+85	°C	
Lead temperature			+245	°C	For 10 seconds
VSWR of antenna			3:1		
ESD protection					
Antenna pad			±250	V	HBM
All other pads			±2	kV	HBM
			±200	V	CDM



**Caution!** ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

## 2.0 Normal Operating Conditions

Unless otherwise noted, Table 2 assumes  $V_{DD}$  is 3.0 V and temperature is 25 °C.

**Table 2 Normal Operating Conditions**

Parameter	Min	Typ	Max	Units	Comments
Operational supply voltage range (between $V_{DD}$ and $V_{SS}$ )	2.75	3.0	3.6	V	Including noise and load regulation
Voltage supply noise			100	mV <sub>p-p</sub>	50 Hz to 2 MHz
Peak current		6		mA	Searching for network, typically 150 ms on and 2850 ms in doze*
Power amplifier enabled		18	12	mA	Mote boot, see section 6.0
Power amplifier enabled			24	mA	TX, 5 ms maximum
Power amplifier disabled		7		mA	TX, 5 ms maximum, +85 °C, 3.3 V
Reset			1.25	mA	TX, 5 ms maximum $\overline{RST}$ asserted
Operating temperature range	-40		+85	°C	
Maximum allowed temperature ramp during operation			8	°C/min	-40 °C to +85 °C
Operating relative humidity	10		90	% RH	Non-condensing

\* The duration of doze time and “on” time is determined by the joinDutyCycle command in the mote serial API. Refer to the *SmartMesh IA-510 Mote Serial API Guide* for details.

Unless otherwise noted, Table 3 assumes  $V_{DD}$  is 3.0 V and temperature is 25 °C.

**Table 3 DN2510 Current Consumption**

Parameter	Min	Typ	Max	Units	Comments
Transmit					
Power amplifier enabled		18		mA	
Power amplifier disabled		7		mA	
Receive		6		mA	

### 3.0 Electrical Specifications

**Table 4 Device Load**

Parameter	Min	Typ	Max	Units	Comments
Total capacitance			0.5	μF	
Total inductance			84	nH	

Unless otherwise noted,  $V_{DD}$  is 3.0 V and temperature is -40 °C to +85 °C.

**Table 5 Digital I/O Type 1**

Digital Signal	Min	Typ	Max	Units	Comments
$V_{IL}$ (low-level input voltage)	-0.3		0.6	V	
$V_{IH}$ (high-level input voltage)	$0.8 \times V_{DD}$		$V_{DD} + 0.3$	V	
$V_{OL}$ (low-level output voltage)			0.4	V	
$V_{OH}$ (high-level output voltage)	2.4			V	
Digital current*					
Output source (single pin)		3.7		mA	25 °C
Output sink (single pin)		2.0		mA	25 °C
Input leakage current		50		nA	

\* This current level guarantees that the output voltage meets  $V_{OH}$  and  $V_{OL}$  specifications above.

**Table 6 Digital I/O Type 2**

Digital Signal	Min	Typ	Max	Units	Comments
$V_{IL}$ (low-level input voltage)	-0.3		0.6	V	
$V_{IH}$ (high-level input voltage)	$0.8 \times V_{DD}$		$V_{DD} + 0.3$	V	
$V_{OL}$ (low-level output voltage, multifunction I/O configured as output)	-0.3		0.6	V	$I_{OL} < 0.6$ mA, 85 °C
$V_{OH}$ (high-level output voltage, multifunction I/O configured as output)	$V_{DD} - 0.6$		$V_{DD}$	V	$I_{OH} > -0.4$ mA, 85 °C
Digital current*					
Output source (single pin, multifunction I/O configured as output)		0.4		mA	25 °C
Output sink (single pin, multifunction I/O configured as output)		0.6		mA	25 °C
Input leakage current		50		nA	25 °C

\* This current level guarantees that the output voltage meets  $V_{OH}$  and  $V_{OL}$  specifications above.

**Table 7 Digital I/O Type 3**

Digital Signal	Min	Typ	Max	Units	Comments
V <sub>IL</sub> (low-level input voltage)	-0.3		0.6	V	
V <sub>IH</sub> (high-level input voltage)	2.0		V <sub>DD</sub> + 0.3	V	
V <sub>OL</sub> (low-level output voltage)			0.4	V	
V <sub>OH</sub> (high-level output voltage)	V <sub>DD</sub> - 0.2			V	
Digital current*					
Output source (single pin)		100		μA	25 °C
Output sink (single pin)		1.6		mA	25 °C
Input leakage current		50		nA	25 °C

\* This current level guarantees that the output voltage meets V<sub>OH</sub> and V<sub>OL</sub> specifications above.

## 4.0 Radio

### 4.1 Detailed Radio Specifications

**Table 8 Radio Specifications**

Parameter	Min	Typ	Max	Units	Comments
Operating frequency	2.4000		2.4835	GHz	
Number of channels		15			
Channel separation		5		MHz	
Occupied channel bandwidth		2.7		MHz	At -20 dBc
Frequency Accuracy	-40		+40	ppm	
Modulation					IEEE 802.15.4 DSSS
Raw data rate		250		kbps	
Receiver operating maximum input level		0		dBm	
Receiver sensitivity		-92.5		dBm	At 50% PER, V <sub>DD</sub> = 3 V, 25 °C
		-90		dBm	At 1% PER, V <sub>DD</sub> = 3 V, 25 °C
Output power, conducted					
Power amplifier enabled		+8		dBm	V <sub>DD</sub> = 3 V, 25 °C
Power amplifier disabled		-2		dBm	V <sub>DD</sub> = 3 V, 25 °C
Range*					
Power amplifier enabled:					
Indoor <sup>†</sup>		100		m	25 °C, 50% RH, +2 dBi omni-directional antenna
Outdoor <sup>†</sup>		300		m	
Free space		1200		m	
Power amplifier disabled:					
Indoor <sup>†</sup>		25		m	
Outdoor <sup>†</sup>		200		m	
Free space		350		m	

\* Actual RF range performance is subject to a number of installation-specific variables including, but not restricted to ambient temperature, relative humidity, presence of active interference sources, line-of-sight obstacles, near-presence of objects (for example, trees, walls, signage, and so on) that may induce multipath fading. As a result, actual performance varies for each instance.

<sup>†</sup> 1 meter above ground.

## 4.2 Antenna Specifications

The antenna must meet specifications in Table 9.

**Table 9 Antenna Specifications**

Parameter	Value
Frequency range	2.4–2.4835 GHz
Impedance	50 $\Omega$
Maximum VSWR	3:1

When the mote is placed inside an enclosure, the antenna should be mounted such that the radiating portion of the antenna protrudes from the enclosure and connected using a coaxial cable. For optimum performance, allow the antenna to be positioned vertically when installed.

## 5.0 Pinout

The following is the pinout for the 12 mm x 12 mm LGA package. For pin numbering, refer to the bottom view of the mechanical drawing shown in section 8.1.

**Note:** All unused input pins must be driven to an active state to avoid excess leakage and undesired operation. Leakage due to floating inputs can be substantially greater than the average power consumption.

**Table 10 Pinout Assignments for the DN2510**

Pin Number	Pin Name	Description	Type	Direction	Pin State in Deep Sleep <sup>†</sup>
1	V <sub>DD</sub>	Power	–	In	–
2	<i>Reserved</i>	No connect	–	–	–
3	V <sub>SS</sub>	Ground	–	In	–
4	Antenna	Antenna RF connection	–	I/O	–
5	V <sub>SS</sub>	Ground	–	In	–
6	<i>Reserved</i>	No connect	–	–	–
7	<i>Reserved</i>	No connect	–	–	–
8	<i>Reserved</i>	No connect	–	–	–
9	GP8	Functionality set by Mode pin B	1	I/O	V <sub>DD</sub>
10	V <sub>DD</sub>	Flash Power	–	In	–
11	$\overline{\text{RST}}$	External reset	1	In	–
12	<i>Reserved</i>	No connect	–	–	–
13	<i>Reserved</i>	No connect	–	–	–
14	<i>Reserved</i>	No connect	–	–	–
15	<i>Reserved</i>	No connect	–	–	–
16	V <sub>SS</sub>	Ground	–	In	–
17	$\overline{\text{FLASH\_P\_EN}}$	Active low flash power enable	1	In*	–
18	$\overline{\text{SPI\_CS}}$	Active low flash chip select	3	In*	–
19	<i>Reserved</i>	No connect	–	–	–
20	GP1	Functionality set by Mode pin B	2	I/O	V <sub>DD</sub>
21	GP2 / Mode pin B	Mode pin B	2	I/O	–
22	GP3	Functionality set by Mode pin B	2	I/O	–
23	GP4	Functionality set by Mode pin B	2	I/O	–
24	GP5	Functionality set by Mode pin B	2	I/O	V <sub>DD</sub>
25	V <sub>SS</sub>	Ground	–	In	–
26	GP6	Functionality set by Mode pin B	2	I/O	–
27	<i>Reserved</i>	No connect	–	–	–

Pin Number	Pin Name	Description	Type	Direction	Pin State in Deep Sleep <sup>†</sup>
28	Reserved	No connect	–	–	–
29	GP7	Functionality set by Mode pin B	1	I/O	V <sub>DD</sub>
30	Reserved	No connect	–	–	–
31	SCK	SPI clock	3	In*	–
32	MOSI	SPI master out slave in serial data	3	In*	–
33	MISO	SPI master in slave out serial data	3	Out*	V <sub>DD</sub> **
34	Reserved	No connect	–	–	–
35	V <sub>SS</sub>	Ground	–	In	–
36	Reserved	No connect	–	–	–
37	Reserved	No connect	–	–	–
38	Reserved	No connect	–	–	–
39	V <sub>SS</sub>	Ground	–	In	–
40	V <sub>DD</sub>	Power	–	In	–

\* The direction associated with the flash interface are defined when the device is held in reset and is intended solely for the use of in-circuit programming of the device. Following reset all inputs will become outputs and must not be driven externally.

\*\* Weakly pulled to V<sub>DD</sub>.

† Deep sleep is the lowest possible power state, with V<sub>DD</sub> and GND connected. The mote microprocessor and radio are inactive, and the mote must be awakened using the /RST signal (for more information see the lowPowerSleep command in the IA-510 Mote Serial API Guide).

## 6.0 Mote Boot Up

### 6.1 Power-on Sequence

The DN2510 has internal power-on reset circuits that ensure that the mote will properly boot. However, for the power-on reset circuitry to function properly the external power supply must meet the timing shown in Figure 1 and specified in Table 11.

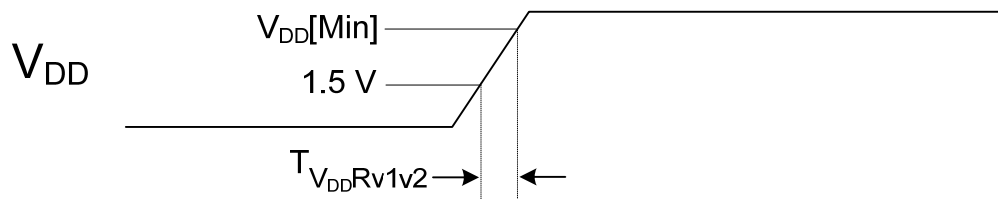


Figure 1 External Power Supply Timing Requirement

The following reset sequence (shown in Figure 2 and specified in Table 11) is required for external power supplies that fail to meet the requirement above.

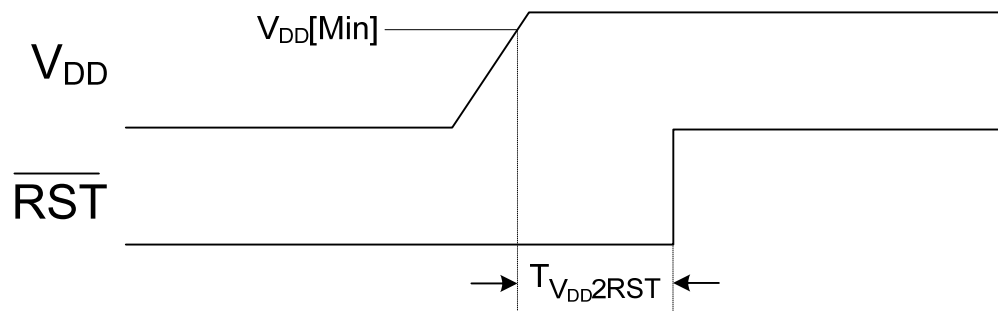


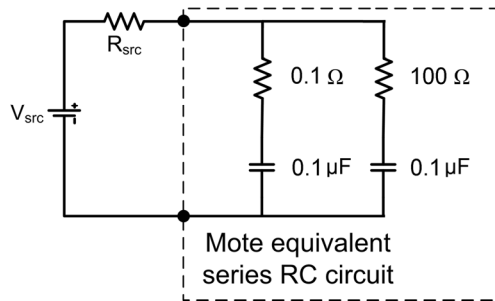
Figure 2 Power-on Sequence

**Table 11 Power-on Sequence**

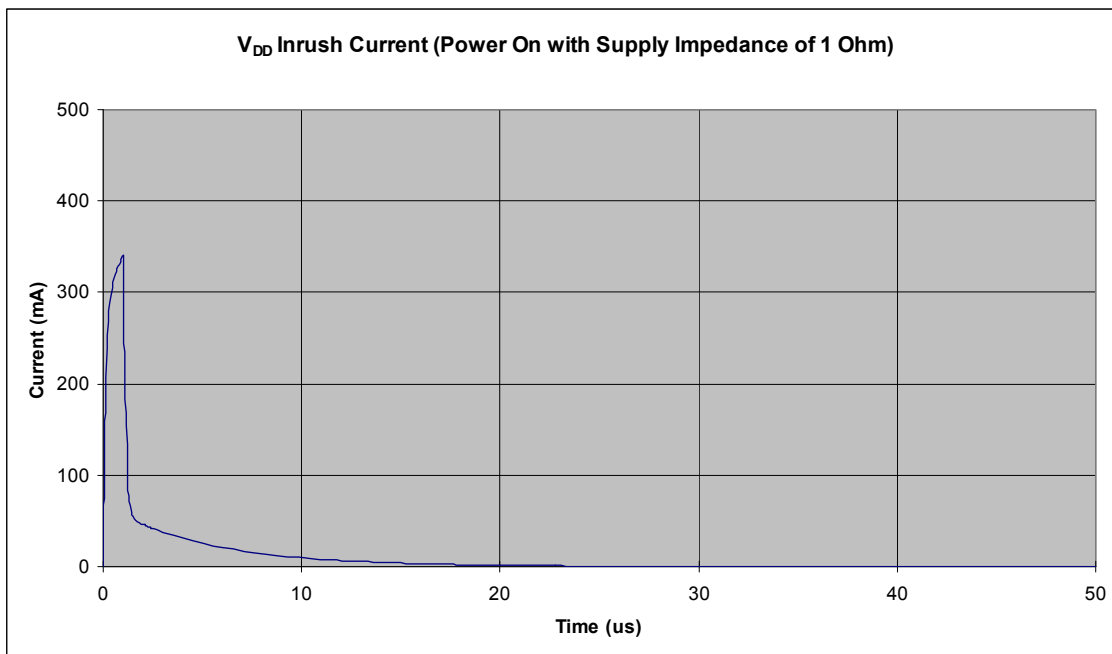
Parameter	Min	Typ	Max	Units	Comments
TV <sub>DD2RST</sub>	125			μs	
TV <sub>DDRV1v2</sub>			1	ms	
$\overline{\text{RST}}$ pulse width	125			μs	Reset timing

## 6.2 Inrush Current

During power on, the mote can be modeled via lumped impedances, as shown in Figure 3. With a source impedance ( $R_{\text{src}}$ ) of 1 Ω, the inrush current on the mote appears as shown in Figure 4.



**Figure 3 DN2510 Equivalent Series RC Circuit**



**Figure 4 V<sub>DD</sub> Inrush Current**

## 6.3 Mote Boot Sequence

Following the negation of  $\overline{\text{RST}}$  the mote completes its boot up process by loading and decrypting the application image and loading the operating parameters. During the boot process, the mote’s output signals are not actively driven and the input signals are ignored.

The DN2510 supports two mote boot modes: standard boot and low current boot. Standard boot is optimized for quick boot time. Low current boot lowers the average current but at a longer boot time. The mote boot mode is determined by the software executable loaded onto the DN2510.

## 6.3.1 Standard Boot

When the DN2510 operates in standard boot, the time between the mote power up and the serial interface availability is defined as  $t_{boot\_delay}$  and specified in Table 12 Standard Boot Sequence below. The peak current during mote boot is specified under Peak Current in Table 2.

**Table 12 Standard Boot Sequence**

Parameter	Min	Typ	Max	Units	Comments
$t_{boot\_delay}$			6	s	The time between mote power up and serial interface availability.

## 6.3.2 Low Current Boot

When operating in Low Current Boot, the DN2510 lowers average current consumption by spreading the boot operation over a longer time. This mode is intended to support systems with supplies having a maximum DC current less than the peak current required by the DN2510. These systems must store enough charge to maintain the supply through the DN2510's peak current consumption. For more information, contact your Dust Networks applications engineer.

# 7.0 Interfaces

## 7.1 Reset Pin

The /RST input pin is internally pulled up. Connecting it is optional; however, in applications operating in the presence of EMI, /RST should be actively driven high. When driven low, the mote hardware is in reset. Note that the mote may also be reset using the mote reset command (0x08). For requirements on reset timing, see section 6.1.

The DN2510 is a highly sophisticated device and Dust Networks recommends doing resets gracefully. If the device is in the network, a disconnect command (0x07) should be issued before the /RST signal is asserted. This will result in the device rebooting and sending the "boot" event.

The /RST signal may then be asserted since the device is not in the network.

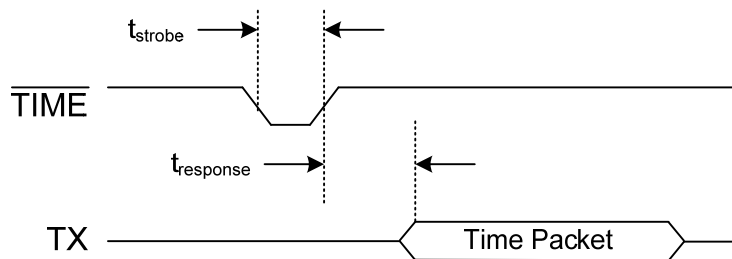
Refer to the *SmartMesh IA-510 DN2510 Integration Guide* for recommendations on how to connect to the /RST pin, including voltage supervision. For detailed information about mote serial commands, refer to the *SmartMesh IA-510 Mote Serial API Guide*.

## 7.2 Timestamps

The DN2510 has the ability to deliver network-wide synchronized timestamps. The DN2510 sends a time packet (as described in the *SmartMesh IA-510 Mote Serial API Guide*) through its serial interface when one of the following occurs:

- Mote receives an HDLC request to read time
- The  $\overline{\text{TIME}}$  signal is asserted

The  $\overline{\text{TIME}}$  pin is optional and has the advantage of being more accurate. The value of the timestamp is taken within approximately 1 ms of receiving a  $\overline{\text{TIME}}$  signal activation. If the HDLC request is used, due to packet processing the value of the timestamp may be captured several milliseconds after receipt of the packet. Refer to the *IA-510 Mote Serial API Guide* for more information on timestamps.



**Figure 6 Operation of  $\overline{\text{TIME}}$  Pin**

**Table 14**  $\overline{\text{TIME}}$  Timing Values

Variable	Description	Min	Max	Units
$t_{\text{strobe}}$	$\overline{\text{TIME}}$ strobe pulse width	125		$\mu\text{s}$
$t_{\text{response}}$	Negation of Time strobe to start of time packet		100	ms

### 7.3 SPI Mote Programming Interface

The DN2510 features a Serial Peripheral Interface (SPI) for programming the mote software during the OEM manufacturing process. With this mote programming capability, OEMs may exercise revision control of the mote software in their final product.

OEM designs may include a connection to the SPI pins ( $\overline{\text{FLASH\_P\_EN}}$ ,  $\overline{\text{SPI\_CS}}$ , SCK, MOSI, MISO,  $\overline{\text{RST}}$ ,  $V_{\text{SS}}$ ) suitable for their needs. Note that the mote SPI connection is for programming purposes only, and should be left floating during normal operation. For design-critical layout and SPI programmer information, refer to the *DN2510 Integration Guide*.

### 7.4 Settable I/O Modes

The DN2510 offers a choice of two I/O modes. The functionality of the interface will be determined by the setting of Mode pin B whose pinout is described in 5.0 Pinout.

**Table 15** Mode Pin Settings

Pin	Mode 1	Mode 3
Mode pin B	Externally tied low	Externally tied high

All modes provide a means of transmitting and receiving serial data through the wireless network, as well as a command interface that provides synchronized time stamping, local configuration, and diagnostics.

Mode 1 implements an 8-bit, no parity, 9600 bps three, four, or five-signal serial interface with bidirectional packet-level flow control operating at 9600 bps. In certain OEM designs, one or two of the serial handshake signals may be optional for reduced pin count. Please refer to detailed descriptions of signals.

Mode 3 implements an 8-bit, no parity, 115.2 kbps baud five-signal serial interface with bidirectional packet-level flow control and byte-level flow control in the mote-to-microprocessor direction only.

Pin assignments for GP1 through GP8 are shown in Table 16.

**Table 16** General Purpose Pin Functionality by Mode

Pin Name	Mode 1	Mode 3
GP1	$\overline{\text{MT\_RTS}}$	$\overline{\text{MT\_RTS}}$
GP2	Mode pin B	Mode pin B
GP3	$\overline{\text{SP\_CTS}}$	$\overline{\text{SP\_CTS}}$ *
GP4	$\overline{\text{TIME}}$	$\overline{\text{TIME}}$
GP5	TX	TX
GP6	RX	RX
GP7	$\overline{\text{MT\_CTS}}$	$\overline{\text{MT\_CTS}}$
GP8	<i>Reserved</i>	<i>Reserved</i>

\* Behavior of the  $\overline{\text{SP\_CTS}}$  signal varies between Mode 1 and Mode 3.

## 7.4.1 Mode 1: Three/Four/Five-signal Serial Interface (9600 bps)

The DN2510 mode 1 provides a three, four, or five-signal serial interface that is optimized for low-powered embedded applications (and in certain designs may provide a low pin count serial solution). The mode 1 serial interface is comprised of the data pins (TX, RX) as well as handshake pins ( $\overline{\text{MT\_RTS}}$ ,  $\overline{\text{MT\_CTS}}$ ,  $\overline{\text{SP\_CTS}}$ ) used for bidirectional flow control. The  $\overline{\text{MT\_RTS}}$  signal is ideal for designs where the microprocessor requires extra time to prepare to receive a packet (for example, the OEM microprocessor sleeps periodically, but requires a wake-up signal prior to receiving a packet). Refer to Table 17 for information on each handshake pin, including details on which pins are optional.

**Table 17 Mode 1 Pin Usage**

Pin	I/O	Usage
RX	Input	Serial data moving from the microprocessor to the mote.
TX	Output	Serial data moving from the mote to the microprocessor.
$\overline{\text{MT\_RTS}}$	Output	$\overline{\text{MT\_RTS}}$ provides a mechanism to wake up the microprocessor in order to receive a packet. This signal is asserted when the mote is ready to send a serial packet. The signal stays low until the $\overline{\text{SP\_CTS}}$ signal from the microprocessor is detected low by the mote (indicating readiness to receive a packet) or the $t_{\overline{\text{MT\_RTS}} \text{ to } \overline{\text{SP\_CTS}}}$ timeout defined in Section 7.4.3 expires. If $\overline{\text{MT\_RTS}}$ times out, it will de-assert $\overline{\text{MT\_RTS}}$ , wait for $t_{\overline{\text{MT\_RTS}} \text{ retry}}$ and then re-assert $\overline{\text{MT\_RTS}}$ to attempt to send the serial packet again (see Figure 10). $\overline{\text{MT\_RTS}}$ may be ignored by the microprocessor only if $\overline{\text{SP\_CTS}}$ always stays low.
$\overline{\text{SP\_CTS}}$	Input	$\overline{\text{SP\_CTS}}$ provides packet-level flow control for packets transferred from the mote to the microprocessor. When the microprocessor is capable of receiving a packet it should assert the $\overline{\text{SP\_CTS}}$ signal. $\overline{\text{SP\_CTS}}$ may be externally tied low (reducing pin count) only if the microprocessor is always ready to receive a serial packet.
$\overline{\text{MT\_CTS}}$	Output	$\overline{\text{MT\_CTS}}$ provides packet-level flow control for packets transferred from the microprocessor to the mote that are destined for transfer over the network. Upon reset, following boot the mote will negate $\overline{\text{MT\_CTS}}$ until the mote establishes a wireless network connection. During operation, the mote will negate $\overline{\text{MT\_CTS}}$ if the mote does not have sufficient buffering to accept another packet. $\overline{\text{MT\_CTS}}$ will also remain high if the mote is not part of the network. The microprocessor must check that the $\overline{\text{MT\_CTS}}$ pin is low before initiating each serial packet for wireless transmission. Note that the mote may receive local serial packets at any time regardless of the $\overline{\text{MT\_CTS}}$ state. (For a list of local commands, see the <i>SmartMesh IA-510 Mote Serial API Guide</i> .)
$\overline{\text{TIME}}$	Input	The $\overline{\text{TIME}}$ pin can be used for triggering a timestamp packet. Its usage is optional.

## 7.4.2 Mode 3: Five-signal Serial Interface (115.2 kbps)

The DN2510 mode 3 provides a five-signal serial interface with byte-level flow control on transfers from the mote to the microprocessor. The mode 3 serial interface is comprised of the data pins (TX, RX) as well as handshake pins ( $\overline{\text{MT\_RTS}}$ ,  $\overline{\text{MT\_CTS}}$ ,  $\overline{\text{SP\_CTS}}$ ) used for bidirectional flow control. The  $\overline{\text{MT\_RTS}}$  signal is ideal for designs where the microprocessor requires extra time to prepare to receive a packet (for example, the OEM microprocessor sleeps periodically, but requires a wake-up signal prior to receiving a packet). In order to support 115.2 kbps the microprocessor must include two framing bytes, 0x7E, at the start of each packet sent from the microprocessor to the mote. Refer to Table 18 for information on each handshake pin, including details on which of those pins are optional.

**Table 18 Mode 3 Pin Usage**

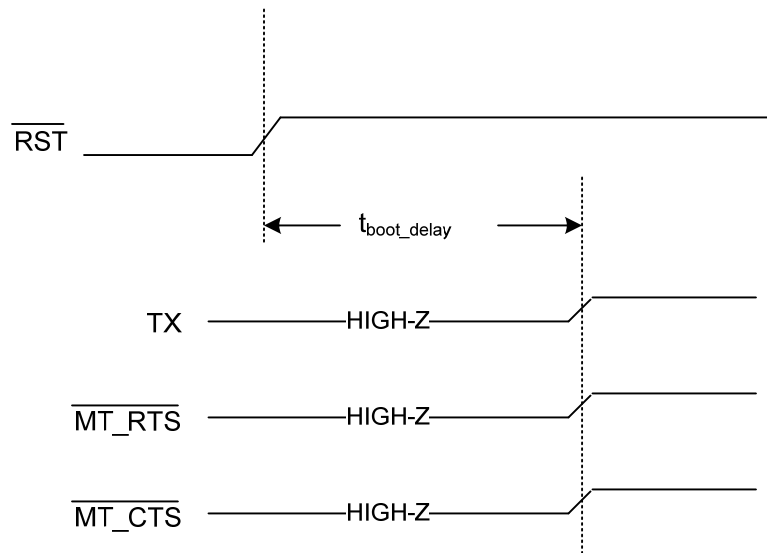
Pin	I/O	Usage
RX	Input	Serial data moving from the microprocessor to the mote.
TX	Output	Serial data moving from the mote to the microprocessor.
$\overline{\text{MT\_RTS}}$	Output	$\overline{\text{MT\_RTS}}$ provides a mechanism to wake up the microprocessor in order to receive a packet. This signal is asserted when the mote is ready to send a serial packet. The signal stays low until the $\overline{\text{SP\_CTS}}$ signal from the microprocessor is detected low by the mote (indicating readiness to receive a packet) or the $t_{\text{MT\_RTS to SP\_CTS}}$ timeout defined in Section 7.4.3 expires. If $\overline{\text{MT\_RTS}}$ times out, it will de-assert $\overline{\text{MT\_RTS}}$ , wait for $t_{\text{MT\_RTS retry}}$ and then re-assert $\overline{\text{MT\_RTS}}$ to attempt to send the serial packet again (see Figure 10).
$\overline{\text{SP\_CTS}}$	Input	$\overline{\text{SP\_CTS}}$ provides byte-level flow control for packets transferred from the mote to the microprocessor. When the microprocessor is capable of receiving a packet it should assert the $\overline{\text{SP\_CTS}}$ signal. In mode 3, byte-level flow control is achieved by having the microprocessor negate and then reassert the $\overline{\text{SP\_CTS}}$ signal following the receipt of each byte. The mote will begin transmission of the next byte after detecting the reassertion of $\overline{\text{SP\_CTS}}$ .
$\overline{\text{MT\_CTS}}$	Output	$\overline{\text{MT\_CTS}}$ provides packet-level flow control for packets transferred from the microprocessor to the mote that are destined for transfer over the network. Upon reset, following boot the mote will negate $\overline{\text{MT\_CTS}}$ until the mote establishes a wireless network connection. During operation, the mote will negate $\overline{\text{MT\_CTS}}$ if the mote does not have sufficient buffering to accept another packet. $\overline{\text{MT\_CTS}}$ will also remain high if the mote is not part of the network. The microprocessor must check that the $\overline{\text{MT\_CTS}}$ pin is low before initiating each serial packet for wireless transmission.  Note that the mote may receive local serial packets at any time regardless of the $\overline{\text{MT\_CTS}}$ state. (For a list of local commands, see the <i>SmartMesh IA-510 Mote Serial API Guide</i> .)
$\overline{\text{TIME}}$	Input	The $\overline{\text{TIME}}$ pin can be used for triggering a timestamp packet. Its usage is optional.

### 7.4.3 UART AC Timing

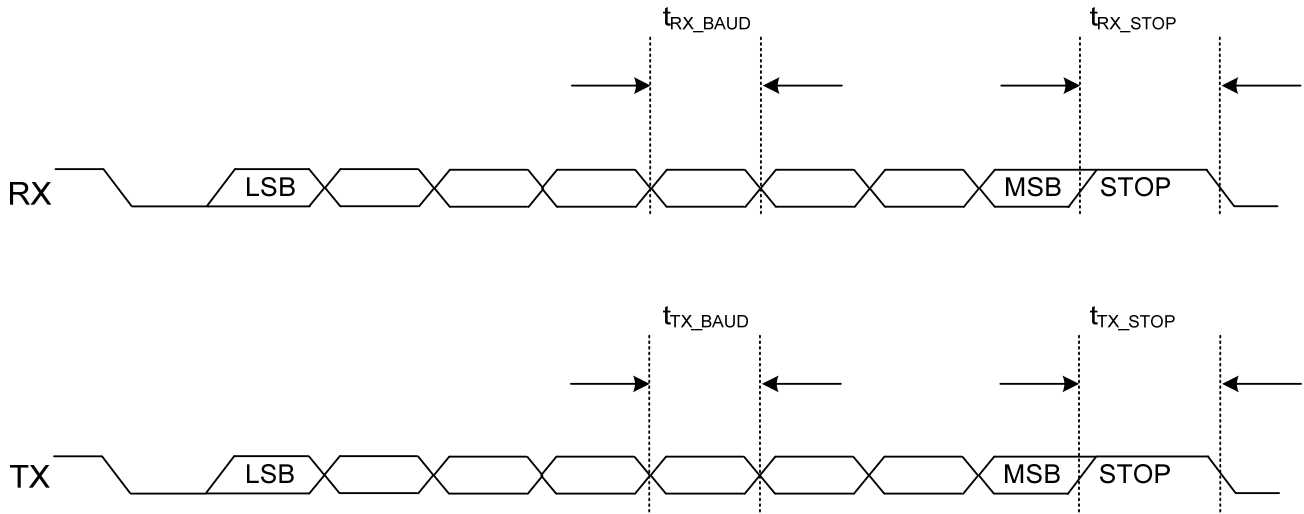
**Table 19 UART Timing Values**

Variable	Description	Min	Max	Units
$t_{\text{RX\_BAUD}}$	Deviation from baud rate	-2	+2	%
$t_{\text{RX\_STOP}}$	Number of stop bits (9600 bps)	1		bit period
$t_{\text{RX\_STOP}}$	Number of stop bits (115.2 kbps)	1.5		bit period
$t_{\text{TX\_BAUD}}$	Deviation from baud rate	-1	+1	%
$t_{\text{TX\_STOP}}$	Number of stop bits	1		bit period
$t_{\text{SP\_CTS to MT\_RTS}}$	Assertion of $\overline{\text{SP\_CTS}}$ to negation of $\overline{\text{MT\_RTS}}$	0	10	ms
$t_{\text{MT\_RTS to SP\_CTS}}$	Assertion of $\overline{\text{MT\_RTS}}$ to assertion of $\overline{\text{SP\_CTS}}$		500	ms
$t_{\text{MT\_RTS retry}}$	Time from a $\overline{\text{MT\_RTS}}$ timeout to the retry.		500	ms
$t_{\text{SP\_CTS to TX}}$	Assertion of $\overline{\text{SP\_CTS}}$ to start of byte	0	10	ms
$t_{\text{TX to SP\_CTS}}$	Start of byte to negation of $\overline{\text{SP\_CTS}}$	1		bit period
$t_{\text{SP\_CTS ack PW}}$	Negation pulse width of $\overline{\text{SP\_CTS}}$	500		ns
$t_{\text{diag\_ack\_timeout}}^*$	The mote responds to all requests within this time.		125	ms
$t_{\text{interbyte\_timeout}}$	Falling edge of TX start bit to falling edge of $\overline{\text{SP\_CTS}}$ (Mode 3 only)		7.1	ms
$t_{\text{interpacket\_delay}}$	The sender of an HDLC packet must wait at least this amount of time before sending another packet	20		ms

\* For more information about supported requests and details on when  $t_{\text{diag\_ack\_timeout}}$  applies, refer to the *SmartMesh IA-510 Mote Serial API Guide*.



**Figure 7 Power-on Sequence** (see section 6.3 for value of  $t_{\text{boot\_delay}}$ )



**Figure 8 Byte-level Timing**

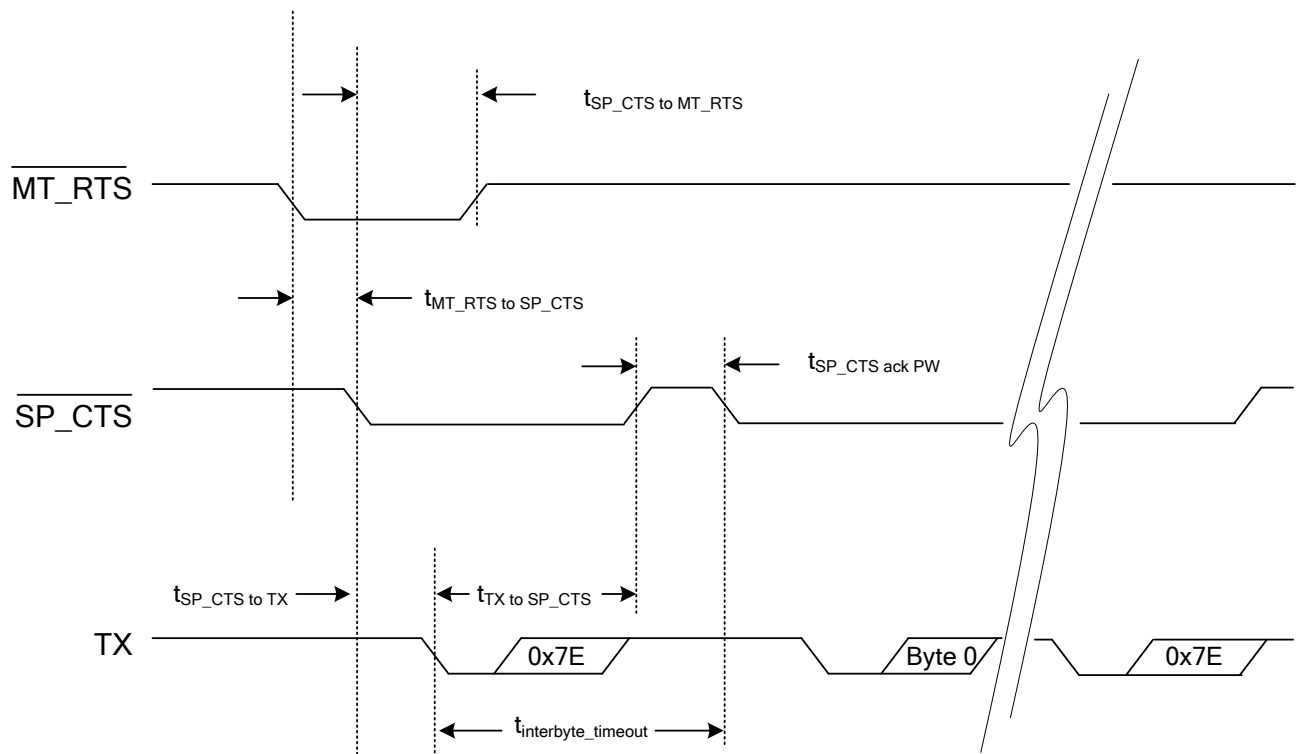


Figure 9 Flow Control Timing

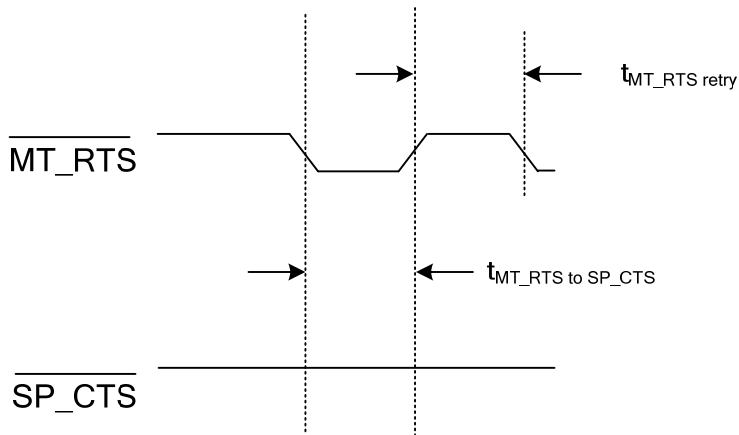


Figure 10  $\overline{\text{MT\_RTS}}$  Timeout Behavior

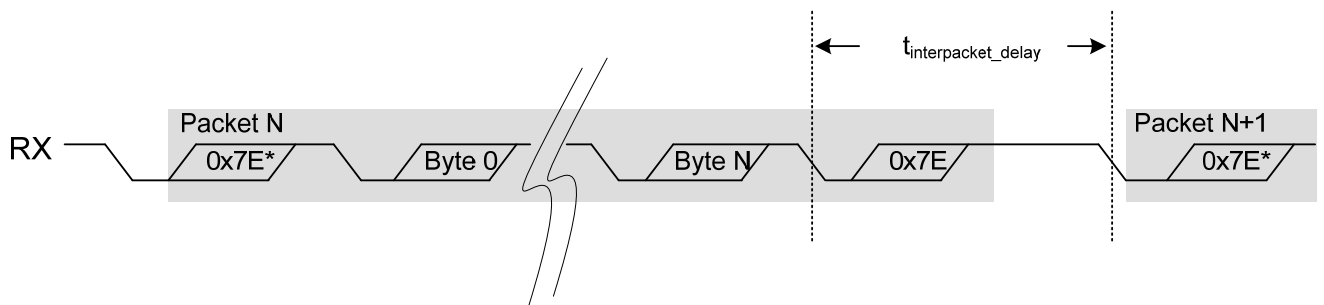


Figure 11 Packet Timing

\* For Mode 3 (115.2 kbps) the framing byte, 0x7E, must be repeated at the start of each packet set to the DN2510.



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## 9.0 Regulatory and Standards Compliance

The DN2510 has achieved modular radio certification on a reference design for the United States, Canada, and the EU.

### 9.1 Compliance to Restriction of Hazardous Substances (RoHS)

Restriction of Hazardous Substances (RoHS) is a directive that places maximum concentration limits on the use of cadmium (Cd), lead (Pb), hexavalent chromium (Cr+6), mercury (Hg), Polybrominated Biphenyl (PBB) and Polybrominated Diphenyl Ethers (PBDE). Dust Networks is committed to meeting the requirements of the European Community directive 2002/95/EC.

This product has been specifically designed to utilize RoHS compliant materials and to eliminate, or reduce, the use of restricted materials to comply with 2002/95/EC.

The Dust Networks RoHS compliant design features include:

- RoHS compliant solder for solder joints
- RoHS compliant base metal alloys
- RoHS compliant precious metal plating
- RoHS compliant cable assemblies and connector choices
- Lead-Free LGA Package
- Halogen-Free Mold Compound
- RoHS Compliant and 245°C Re-flow Compatible

**NOTE:** Dust Network customers may elect to use certain types of lead-free solder alloys in accordance with the European Community directive 2002/95/EC. Depending on the type of solder paste chosen, a corresponding process change to optimize reflow temperatures may be required.

### 9.2 Encryption Cipher

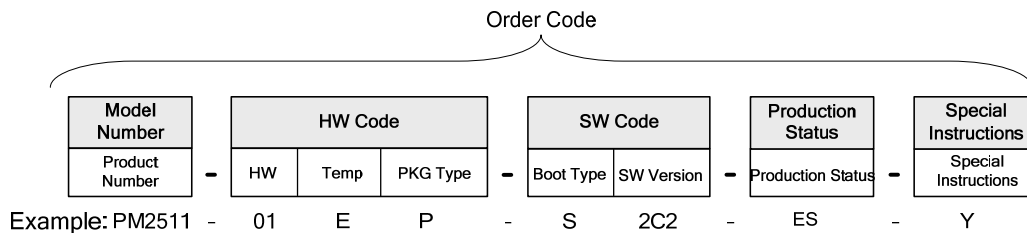
The DN2510's 128-bit Advanced Encryption Standard (AES) cipher has been certified compliant to the United States National Institute of Standards and Technology (NIST) FIPS-197 (NIST certificate number, AES: 1437). To view the FIPS-197 validation list, go to: <http://csrc.nist.gov/groups/STM/cavp/documents/aes/aesval.html>

## 10.0 Related Documentation

- *SmartMesh IA-510 DN2510 Integration Guide*
- *SmartMesh IA-510 Mote Serial API Guide*

## 11.0 Ordering Information

This section explains Dust Networks' order code format. The product order code specifies the model number, software code, production status, and any special instructions for the product. Table 21 describes the order code options. *Note that not all options are valid for every product.* Please contact your Dust Networks Sales Representative for specific product order code information.



**Table 21 Order Code Descriptions**

<b>Code Type</b>	<b>Description</b>
Product Number	Product number
HW	Hardware revision
Temp	Temperature: C = Commercial E = Extended industrial H = High temperature industrial Z = Software only order
PKG Type	Package type: Q = QFN L = LGA P = PCA E = Packaged products K = Development or evaluation kit Z = Software only order
Boot Type	Boot type: S = Standard boot L = Low-current boot Z = Hardware only order
SW Version	Software version
Production Status	ES = Engineering sample Empty = Production
Special Instructions	Y = Special instructions Empty = No special instructions

**Contact Information:**

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**Email:** [sales@dustnetworks.com](mailto:sales@dustnetworks.com)

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Document Status	Product Status	Definition
Advanced Information	Planned or under development	This datasheet contains the design specifications for product development. Dust Networks reserves the right to change specifications in any manner without notice.
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